CLAIMS

What is claimed is:

1) A circuit for improving noise tolerance in multi-threaded memory circuits comprising:

(a) a first PFET with a source, drain, and gate;

(b) a second PFET with a source ,drain , and gate;

(c) a first memory cell connected to VDD and GND, with a receiving input, an output, and a control input;

(d) a second memory cell connected to VDD and GND, with a receiving input, an output, and a control input;

(e) a first transfer gate with an input, a first control input, a second control input and an output;

(f) a second transfer gate with an input, a first control input, a second control input and an output;

(g) wherein the gate of the first PFET is connected to the output of the first memory cell, the drain of the first PFET is connected to the receiving input of the first memory cell, and the source of the first PFET is connected to the control input of the first memory cell;

(h) wherein the gate of the second PFET is connected to the output of the second memory cell, the drain of the second PFET is connected to the receiving input of the second memory cell, and the source of the second PFET is connected to the control input of the second memory cell;

(i) wherein the output of the first transfer gate is connected to the receiving input of the first memory cell and the drain of the first PFET, the first control input of the first transfer gate is connected to a first control signal, the second control input of the first transfer gate is connected to a second control signal and the input of the first transfer gate is connected to a dataline and the input of the second transfer gate;

(j) wherein the output of the second transfer gate is connected to the receiving input of the second memory cell and the drain of the second PFET, the first control input of the second transfer gate is connected to the second control signal, the second control input of the second transfer gate is connected to the first control signal and the input of the second transfer gate is connected to the dataline and the input of the first transfer gate;

(k) such that when the dataline is charged to near GND, the voltage stored on the receiving input of the first memory cell is high, the voltages on the control inputs of the first transfer gate connect the dataline to the receiving input of the first memory cell, and the voltage to the control input of the first and second memory cells is high, the first PFET improves the noise immunity of the first memory cell.

2) The circuit as in Claim 1 wherein the first transfer gate comprises:

(a) a PFET with a source, drain, and gate;

(b) an NFET with a source, drain and gate;

(c) wherein the drain of the PFET and the source of the NFET are connected to the input of the first transfer gate;

(d) wherein the source of the PFET and the drain of the NFET are connected to the output of the first transfer gate;

(e) wherein the gate of the PFET is connected to the first control input of the first transfer gate;

(f) wherein the gate of the NFET is connected to the second control input of the first transfer gate;

(g) wherein the first control signal has the opposite phase of the second control signal.

3) The circuit as in Claim 1 wherein the second transfer gate comprises:

(a) a PFET with a source, drain, and gate;

(b) an NFET with a source, drain and gate;

(c) wherein the drain of the PFET and the source of the NFET are connected to the input of the second transfer gate;

(d) wherein the source of the PFET and the drain of the NFET are connected to the output the second transfer gate;

(e) wherein the gate of the PFET is connected to the first control input of the second transfer gate;

(f) wherein the gate of the NFET is connected to the second control input of the second transfer gate;

(g) wherein the first control signal has the opposite phase of the second control signal.

4) The circuit as in Claim 3 wherein the first transfer gate comprises:

(a) a PFET with a source, drain, and gate;

(b) an NFET with a source, drain and gate;

(c) wherein the drain of the PFET and the source of the NFET are connected to the input of the first transfer gate;

(d) wherein the source of the PFET and the drain of the NFET are connected to the output of the first transfer gate;

(e) wherein the gate of the PFET is connected to the first control input of the first transfer gate;

(f) wherein the gate of the NFET is connected to the second control input of the first transfer gate;

(g) wherein the first control signal has the opposite phase of the second control signal.

5) The circuit as in Claim 1 wherein the first memory cell comprises:

(a) a first PFET with a source, drain, and gate;

(b) a first NFET with a source, drain and gate;

(c) a second PFET with a source, drain, and gate;

(d) a second NFET with a source, drain and gate;

(e) a third NFET with a source, drain and gate;

(f) wherein the sources of first and second PFETs are connected to VDD;

(g) wherein the drain of the first PFET, the gate of the second PFET, and the gate of the second NFET are connected to the output of the first memory cell;

(h) wherein the drain of the second PFET, the gate of the first PFET, and the gate of the first NFET are connected to the receiving input of the first memory cell;

(i) wherein the source of the first NFET is connected to GND;

(j) wherein the source of the second NFET is connected to the drain of the third NFET;

(k) wherein the gate of the third NFET is connected to the control input and the source of the third NFET is connected to GND.

6) The circuit as in Claim 1 wherein the second memory cell comprises:

(a) a first PFET with a source, drain, and gate;

(b) a first NFET with a source, drain and gate;

(c) a second PFET with a source, drain, and gate;

(d) a second NFET with a source, drain and gate;

(e) a third NFET with a source, drain and gate;

(f) wherein the sources of first and second PFETs are connected to VDD;

(g) wherein the drain of the first PFET, the gate of the second PFET, and the gate of the second NFET are connected to the output of the second memory cell;

(h) wherein the drain of the second PFET, the gate of the first PFET, and the gate of the first NFET are connected to the receiving input of the second memory cell;

(i) wherein the source of the first NFET is connected to GND;

(j) wherein the source of the second NFET is connected to the drain of the third NFET;

(k) wherein the gate of the third NFET is connected to the control input and the source of the third NFET is connected to GND.

7) The circuit as in Claim 6 wherein the first memory cell comprises:

(a) a first PFET with a source, drain, and gate;

(b) a first NFET with a source, drain and gate;

(c) a second PFET with a source, drain, and gate;

(d) a second NFET with a source, drain and gate;

(e) a third NFET with a source, drain and gate;

(f) wherein the sources of first and second PFETs are connected to VDD;

(g) wherein the drain of the first PFET, the gate of the second PFET, and the gate of the second NFET are connected to the output of the first memory cell;

(h) wherein the drain of the second PFET, the gate of the first PFET, and the gate of the first NFET are connected to the receiving input of the first memory cell;

(i) wherein the source of the first NFET is connected to GND;

(j) wherein the source of the second NFET is connected to the drain of the third NFET;

(k) wherein the gate of the third NFET is connected to the control input and the source of the third NFET is connected to GND.

8) The circuit as in Claim 7 wherein the first transfer gate comprises:

(a) a PFET with a source, drain, and gate;

(b) an NFET with a source, drain and gate;

(c) wherein the drain of the PFET and the source of the NFET are connected to the input of the first transfer gate;

(d) wherein the source of the PFET and the drain of the NFET are connected to the output of the first transfer gate;

(e) wherein the gate of the PFET is connected to the first control input of the first transfer gate;

(f) wherein the gate of the NFET is connected to the second control input of the first transfer gate;

(g) wherein the first control signal has the opposite phase of the second control signal.

9) The circuit as in Claim 8 wherein the second transfer gate comprises:

(a) a PFET with a source, drain, and gate;

(b) an NFET with a source, drain and gate;

(c) wherein the drain of the PFET and the source of the NFET are connected to the input of the second transfer gate;

(d) wherein the source of the PFET and the drain of the NFET are connected to the output the second transfer gate;

(e) wherein the gate of the PFET is connected to the first control input of the second transfer gate;

(f) wherein the gate of the NFET is connected to the second control input of the second transfer gate;

(g) wherein the first control signal has the opposite phase of the second control signal.

10) A method for improving noise tolerance in multi-threaded memory circuits comprising:

(a) fabricating a first PFET with a source, drain, and gate;

(b) fabricating a second PFET with a source ,drain , and gate;

(c) fabricating a first memory cell connected to VDD and GND, with a receiving input, an output, and a control input;

(d) fabricating a second memory cell connected to VDD and GND, with a receiving input, an output, and a control input;

(e) fabricating a first transfer gate with an input, a first control input, a second control input and an output;

(f) fabricating a second transfer gate with an input, a first control input, a second control input and an output;

(g) wherein the gate of the first PFET is connected to the output of the first memory cell, the drain of the first PFET is connected to the receiving input of the first memory cell, and the source of the first PFET is connected to the control input of the first memory cell;

(h) wherein the gate of the second PFET is connected to the output of the second memory cell, the drain of the second PFET is connected to the receiving input of the second memory cell, and the source of the second PFET is connected to the control input of the second memory cell;

(i) wherein the output of the first transfer gate is connected to the receiving input of the first memory cell and the drain of the first PFET, the first control input of the first transfer gate is connected to a first control signal, the second control input of the first transfer gate is connected to a second control signal and the input of the first transfer gate is connected to a dataline and the input of the second transfer gate;

(j) wherein the output of the second transfer gate is connected to the receiving input of the second memory cell and the drain of the second PFET, the first control input of the second transfer gate is connected to the second control signal, the second control input of the second transfer gate is connected to the first control signal and the input of the second transfer gate is connected to the dataline and the input of the first transfer gate;

(k) such that when the dataline is charged to near GND, the voltage stored on the receiving input of the first memory cell is high, the voltages on the control inputs of the first transfer gate connect the dataline to the receiving input of the first memory cell, and the voltage to the control input of the first and second memory cells is high, the first PFET improves the noise immunity of the first memory cell.

11) The method as in Claim 10 wherein the first transfer gate comprises:

(a) fabricating a PFET with a source, drain, and gate;

(b) fabricating an NFET with a source, drain and gate;

(c) wherein the drain of the PFET and the source of the NFET are connected to the input of the first transfer gate;

(d) wherein the source of the PFET and the drain of the NFET are connected to the output of the first transfer gate;

(e) wherein the gate of the PFET is connected to the first control input of the first transfer gate;

(f) wherein the gate of the NFET is connected to the second control input of the first transfer gate;

(g) wherein the first control signal has the opposite phase of the second control signal.

12) The method as in Claim 10 wherein the second transfer gate comprises:

(a) fabricating a PFET with a source, drain, and gate;

(b) fabricating an NFET with a source, drain and gate;

(c) wherein the drain of the PFET and the source of the NFET are connected to the input of the second transfer gate;

(d) wherein the source of the PFET and the drain of the NFET are connected to the output the second transfer gate;

(e) wherein the gate of the PFET is connected to the first control input of the second transfer gate;

(f) wherein the gate of the NFET is connected to the second control input of the second transfer gate;

(g) wherein the first control signal has the opposite phase of the second control signal.

13) The method as in Claim 12 wherein the first transfer gate comprises:

(a) fabricating a PFET with a source, drain, and gate;

(b) fabricating an NFET with a source, drain and gate;

(c) wherein the drain of the PFET and the source of the NFET are connected to the input of the first transfer gate;

(d) wherein the source of the PFET and the drain of the NFET are connected to the output of the first transfer gate;

(e) wherein the gate of the PFET is connected to the first control input of the first transfer gate;

(f) wherein the gate of the NFET is connected to the second control input of the first transfer gate;

(g) wherein the first control signal has the opposite phase of the second control signal.

14) The method as in Claim 10 wherein the first memory cell comprises:

(a) fabricating a first PFET with a source, drain, and gate;

(b) fabricating a first NFET with a source, drain and gate;

(c) fabricating a second PFET with a source, drain, and gate;

(d) fabricating a second NFET with a source, drain and gate;

(e) fabricating a third NFET with a source, drain and gate;

(f) wherein the sources of first and second PFETs are connected to VDD;

(g) wherein the drain of the first PFET, the gate of the second PFET, and the gate of the second NFET are connected to the output of the first memory cell;

(h) wherein the drain of the second PFET, the gate of the first PFET, and the gate of the first NFET are connected to the receiving input of the first memory cell;

(i) wherein the source of the first NFET is connected to GND;

(j) wherein the source of the second NFET is connected to the drain of the third NFET;

(k) wherein the gate of the third NFET is connected to the control input and the source of the third NFET is connected to GND.

15) The method as in Claim 10 wherein the second memory cell comprises:

(a) fabricating a first PFET with a source, drain, and gate;

(b) fabricating a first NFET with a source, drain and gate;

(c) fabricating a second PFET with a source, drain, and gate;

(d) fabricating a second NFET with a source, drain and gate;

(e) fabricating a third NFET with a source, drain and gate;

(f) wherein the sources of first and second PFETs are connected to VDD;

(g) wherein the drain of the first PFET, the gate of the second PFET, and the gate of the second NFET are connected to the output of the second memory cell;

(h) wherein the drain of the second PFET, the gate of the first PFET, and the gate of the first NFET are connected to the receiving input of the second memory cell;

(i) wherein the source of the first NFET is connected to GND;

(j) wherein the source of the second NFET is connected to the drain of the third NFET;

(k) wherein the gate of the third NFET is connected to the control input and the source of the third NFET is connected to GND.

16) The method as in Claim 15 wherein the first memory cell comprises:

(a) fabricating a first PFET with a source, drain, and gate;

(b) fabricating a first NFET with a source, drain and gate;

(c) fabricating a second PFET with a source, drain, and gate;

(d) fabricating a second NFET with a source, drain and gate;

(e) fabricating a third NFET with a source, drain and gate;

(f) wherein the sources of first and second PFETs are connected to VDD;

(g) wherein the drain of the first PFET, the gate of the second PFET, and the gate of the second NFET are connected to the output of the first memory cell;

(h) wherein the drain of the second PFET, the gate of the first PFET, and the gate of the first NFET are connected to the receiving input of the first memory cell;

(i) wherein the source of the first NFET is connected to GND;

(j) wherein the source of the second NFET is connected to the drain of the third NFET;

(k) wherein the gate of the third NFET is connected to the control input and the source of the third NFET is connected to GND.

17) The method as in Claim 16 wherein the first transfer gate comprises:

(a) a PFET with a source, drain, and gate;

(b) an NFET with a source, drain and gate;

(c) wherein the drain of the PFET and the source of the NFET are connected to the input of the first transfer gate;

(d) wherein the source of the PFET and the drain of the NFET are connected to the output of the first transfer gate;

(e) wherein the gate of the PFET is connected to the first control input of the first transfer gate;

(f) wherein the gate of the NFET is connected to the second control input of the first transfer gate;

(g) wherein the first control signal has the opposite phase of the second control signal.

18) The method as in Claim 17 wherein the second transfer gate comprises:

(a) a PFET with a source, drain, and gate;

(b) an NFET with a source, drain and gate;

(c) wherein the drain of the PFET and the source of the NFET are connected to the input of the second transfer gate;

(d) wherein the source of the PFET and the drain of the NFET are connected to the output the second transfer gate;

(e) wherein the gate of the PFET is connected to the first control input of the second transfer gate;

(f) wherein the gate of the NFET is connected to the second control input of the second transfer gate;

(g) wherein the first control signal has the opposite phase of the second control signal.

19) A circuit for improving noise tolerance in multi-threaded memory circuits comprising:

(a) a first PFET with a source, drain, and gate;

(b) a second PFET with a source ,drain , and gate;

(c) a first memory cell connected to VDD and GND, with a receiving input, an output, and a control input;

(d) a second memory cell connected to VDD and GND, with a receiving input, an output, and a control input;

(e) a first transfer gate with an input, a first control input, a second control input and an output;

(f) a second transfer gate with an input, a first control input, a second control input and an output;

(g) wherein the gate of the first PFET is connected to the output of the first memory cell, the drain of the first PFET is connected to the receiving input of the first memory cell, and the source of the first PFET is connected to the control input of the first memory cell;

(h) wherein the gate of the second PFET is connected to the output of the second memory cell, the drain of the second PFET is connected to the

receiving input of the second memory cell, and the source of the second PFET is connected to the control input of the second memory cell;

(i) wherein the output of the first transfer gate is connected to the receiving input of the first memory cell and the drain of the first PFET, the first control input of the first transfer gate is connected to a first control signal, the second control input of the first transfer gate is connected to a second control signal and the input of the first transfer gate is connected to a dataline and the input of the second transfer gate;

(j) wherein the output of the second transfer gate is connected to the receiving input of the second memory cell and the drain of the second PFET, the first control input of the second transfer gate is connected to the second control signal, the second control input of the second transfer gate is connected to the first control signal and the input of the second transfer gate is connected to the dataline and the input of the first transfer gate;

(k) such that when the dataline is charged to near GND, the voltage stored on the receiving input of the second memory cell is high, the voltages on the control inputs of the second transfer gate connect the dataline to the receiving input of the second memory cell, and the voltage to the control input of the first and second memory cells is high, the second PFET improves the noise immunity of the second memory cell.

20) The circuit as in Claim 19 wherein the first transfer gate comprises:

(a) a PFET with a source, drain, and gate;

(b) an NFET with a source, drain and gate;

(c) wherein the drain of the PFET and the source of the NFET are connected to the input of the first transfer gate;

(d) wherein the source of the PFET and the drain of the NFET are connected to the output of the first transfer gate;

(e) wherein the gate of the PFET is connected to the first control input of the first transfer gate;

(f) wherein the gate of the NFET is connected to the second control input of the first transfer gate;

(g) wherein the first control signal has the opposite phase of the second control signal.

21) The circuit as in Claim 19 wherein the second transfer gate comprises:

(a) a PFET with a source, drain, and gate;

(b) an NFET with a source, drain and gate;

(c) wherein the drain of the PFET and the source of the NFET are connected to the input of the second transfer gate;

(d) wherein the source of the PFET and the drain of the NFET are connected to the output the second transfer gate;

(e) wherein the gate of the PFET is connected to the first control input of the second transfer gate;

(f) wherein the gate of the NFET is connected to the second control input of the second transfer gate;

(g) wherein the first control signal has the opposite phase of the second control signal.

22) The circuit as in Claim 21 wherein the first transfer gate comprises:

(a) a PFET with a source, drain, and gate;

(b) an NFET with a source, drain and gate;

(c) wherein the drain of the PFET and the source of the NFET are connected to the input of the first transfer gate;

(d) wherein the source of the PFET and the drain of the NFET are connected to the output of the first transfer gate;

(e) wherein the gate of the PFET is connected to the first control input of the first transfer gate;

(f) wherein the gate of the NFET is connected to the second control input of the first transfer gate;

(g) wherein the first control signal has the opposite phase of the second control signal.

23) The circuit as in Claim 19 wherein the first memory cell comprises:

(a) a first PFET with a source, drain, and gate;

(b) a first NFET with a source, drain and gate;

(c) a second PFET with a source, drain, and gate;

(d) a second NFET with a source, drain and gate;

(e) a third NFET with a source, drain and gate;

(f) wherein the sources of first and second PFETs are connected to VDD;

(h) wherein the drain of the first PFET, the gate of the second PFET, and the gate of the second NFET are connected to the output of the first memory cell;

(i) wherein the drain of the second PFET, the gate of the first PFET, and the gate of the first NFET are connected to the receiving input of the first memory cell;

(j) wherein the source of the first NFET is connected to GND;

(k) wherein the source of the second NFET is connected to the drain of the third NFET;

(l) wherein the gate of the third NFET is connected to the control input and the source of the third NFET is connected to GND.

24) The circuit as in Claim 19 wherein the second memory cell comprises:

(a) a first PFET with a source, drain, and gate;

(b) a first NFET with a source, drain and gate;

(c) a second PFET with a source, drain, and gate;

(d) a second NFET with a source, drain and gate;

(e) a third NFET with a source, drain and gate;

(f) wherein the sources of first and second PFETs are connected to VDD;

(g) wherein the drain of the first PFET, the gate of the second PFET, and the gate of the second NFET are connected to the output of the second memory cell;

(h) wherein the drain of the second PFET, the gate of the first PFET, and the gate of the first NFET are connected to the receiving input of the second memory cell;

(i) wherein the source of the first NFET is connected to GND;

(j) wherein the source of the second NFET is connected to the drain of the third NFET;

(k) wherein the gate of the third NFET is connected to the control input and the source of the third NFET is connected to GND.

25) The circuit as in Claim 24 wherein the first memory cell comprises:

(a) a first PFET with a source, drain, and gate;

(b) a first NFET with a source, drain and gate;

(c) a second PFET with a source, drain, and gate;

(d) a second NFET with a source, drain and gate;

(e) a third NFET with a source, drain and gate;

(f) wherein the sources of first and second PFETs are connected to VDD;

(g) wherein the drain of the first PFET, the gate of the second PFET, and the gate of the second NFET are connected to the output of the first memory cell;

(h) wherein the drain of the second PFET, the gate of the first PFET, and the gate of the first NFET are connected to the receiving input of the first memory cell;

(i) wherein the source of the first NFET is connected to GND;

(j) wherein the source of the second NFET is connected to the drain of the third NFET;

(k) wherein the gate of the third NFET is connected to the control input and the source of the third NFET is connected to GND.

26) The circuit as in Claim 25 wherein the first transfer gate comprises:

(a) a PFET with a source, drain, and gate;

(b) an NFET with a source, drain and gate;

(c) wherein the drain of the PFET and the source of the NFET are connected to the input of the first transfer gate;

(d) wherein the source of the PFET and the drain of the NFET are connected to the output of the first transfer gate;

(e) wherein the gate of the PFET is connected to the first control input of the first transfer gate;

(f) wherein the gate of the NFET is connected to the second control input of the first transfer gate;

(g) wherein the first control signal has the opposite phase of the second control signal.

27) The circuit as in Claim 26 wherein the second transfer gate comprises:

(a) a PFET with a source, drain, and gate;

(b) an NFET with a source, drain and gate;

(c) wherein the drain of the PFET and the source of the NFET are connected to the input of the second transfer gate;

(d) wherein the source of the PFET and the drain of the NFET are connected to the output the second transfer gate;

(e) wherein the gate of the PFET is connected to the first control input of the second transfer gate;

(f) wherein the gate of the NFET is connected to the second control input of the second transfer gate;

(g) wherein the first control signal has the opposite phase of the second control signal.

28) A method for improving noise tolerance in multi-threaded memory circuits comprising:

(a) fabricating a first PFET with a source, drain, and gate;

(b) fabricating a second PFET with a source ,drain , and gate;

(c) fabricating a first memory cell connected to VDD and GND, with a receiving input, an output, and a control input;

(d) fabricating a second memory cell connected to VDD and GND, with a receiving input, an output, and a control input;

(e) fabricating a first transfer gate with an input, a first control input, a second control input and an output;

(f) fabricating a second transfer gate with an input, a first control input, a second control input and an output;

(g) wherein the gate of the first PFET is connected to the output of the first memory cell, the drain of the first PFET is connected to the receiving input of the first memory cell, and the source of the first PFET is connected to the control input of the first memory cell;

(h) wherein the gate of the second PFET is connected to the output of the second memory cell, the drain of the second PFET is connected to the receiving input of the second memory cell, and the source of the second PFET is connected to the control input of the second memory cell;

(i) wherein the output of the first transfer gate is connected to the receiving input of the first memory cell and the drain of the first PFET, the first control input of the first transfer gate is connected to a first control signal, the second control input of the first transfer gate is connected to a second control signal and the input of the first transfer gate is connected to a dataline and the input of the second transfer gate;

(j) wherein the output of the second transfer gate is connected to the receiving input of the second memory cell and the drain of the second PFET, the first control input of the second transfer gate is connected to the second control signal, the second control input of the second transfer gate is

connected to the first control signal and the input of the second transfer gate is connected to the dataline and the input of the first transfer gate;

(k) such that when the dataline is charged to near GND, the voltage stored on the receiving input of the second memory cell is high, the voltages on the control inputs of the second transfer gate connect the dataline to the receiving input of the second memory cell, and the voltage to the control input of the first and second memory cells is high, the second PFET improves the noise immunity of the second memory cell.

29) The method as in Claim 28 wherein the first transfer gate comprises:

(a) fabricating a PFET with a source, drain, and gate;

(b) fabricating an NFET with a source, drain and gate;

(c) wherein the drain of the PFET and the source of the NFET are connected to the input of the first transfer gate;

(d) wherein the source of the PFET and the source of the NFET are connected to the output of the first transfer gate;

(e) wherein the gate of the PFET is connected to the first control input of the first transfer gate;

(f) wherein the gate of the NFET is connected to the second control input of the first transfer gate;

(g) wherein the first control signal has the opposite phase of the second control signal.

30) The method as in Claim 28 wherein the second transfer gate comprises:

(a) fabricating a PFET with a source, drain, and gate;

(b) fabricating an NFET with a source, drain and gate;

(c) wherein the drain of the PFET and the source of the NFET are connected to the input of the second transfer gate;

(d) wherein the source of the PFET and the drain of the NFET are connected to the output the second transfer gate;

(e) wherein the gate of the PFET is connected to the first control input of the second transfer gate;

(f) wherein the gate of the NFET is connected to the second control input of the second transfer gate;

(g) wherein the first control signal has the opposite phase of the second control signal.

31) The method as in Claim 30 wherein the first transfer gate comprises:

(a) fabricating a PFET with a source, drain, and gate;

(b) fabricating an NFET with a source, drain and gate;

(c) wherein the drain of the PFET and the source of the NFET are connected to the input of the first transfer gate;

(d) wherein the source of the PFET and the drain of the NFET are connected to the output of the first transfer gate;

(e) wherein the gate of the PFET is connected to the first control input of the first transfer gate;

(f) wherein the gate of the NFET is connected to the second control input of the first transfer gate;

(g) wherein the first control signal has the opposite phase of the second control signal.

32) The method as in Claim 28 wherein the first memory cell comprises:

(a) fabricating a first PFET with a source, drain, and gate;

(b)fabricating a first NFET with a source, drain and gate;

(c) fabricating a second PFET with a source, drain, and gate;

(d) fabricating a second NFET with a source, drain and gate;

(e) fabricating a third NFET with a source, drain and gate;

(f) wherein the sources of first and second PFETs are connected to VDD;

(g) wherein the drain of the first PFET, the gate of the second PFET, and the gate of the second NFET are connected to the output of the first memory cell;

(h) wherein the drain of the second PFET, the gate of the first PFET, and the gate of the first NFET are connected to the receiving input of the first memory cell;

(i) wherein the source of the first NFET is connected to GND;

(j) wherein the source of the second NFET is connected to the drain of the third NFET;

(k) wherein the gate of the third NFET is connected to the control input and the source of the third NFET is connected to GND.

33) The method as in Claim 28 wherein the second memory cell comprises:

(a) fabricating a first PFET with a source, drain, and gate;

(c) fabricating a first NFET with a source, drain and gate;

(c) fabricating a second PFET with a source, drain, and gate;

(d) fabricating a second NFET with a source, drain and gate;

(e) fabricating a third NFET with a source, drain and gate;

(f) wherein the sources of first and second PFETs are connected to VDD;

(g) wherein the drain of the first PFET, the gate of the second PFET, and the gate of the second NFET are connected to the output of the second memory cell;

(h) wherein the drain of the second PFET, the gate of the first PFET, and the gate of the first NFET are connected to the receiving input of the second memory cell;

(i) wherein the source of the first NFET is connected to GND;

(j) wherein the source of the second NFET is connected to the drain of the third NFET;

(k) wherein the gate of the third NFET is connected to the control input and the source of the third NFET is connected to GND.

34) The method as in Claim 33 wherein the first memory cell comprises:

(a) fabricating a first PFET with a source, drain, and gate;

(b) fabricating a first NFET with a source, drain and gate;

(c) fabricating a second PFET with a source, drain, and gate;

(d) fabricating a second NFET with a source, drain and gate;

(e) fabricating a third NFET with a source, drain and gate;

(f) wherein the sources of first and second PFETs are connected to VDD;

(g) wherein the drain of the first PFET, the gate of the second PFET, and the gate of the second NFET are connected to the output of the first memory cell;

(h) wherein the drain of the second PFET, the gate of the first PFET, and the gate of the first NFET are connected to the receiving input of the first memory cell;

(i) wherein the source of the first NFET is connected to GND;

(j) wherein the source of the second NFET is connected to the drain of the third NFET;

(k) wherein the gate of the third NFET is connected to the control input and the source of the third NFET is connected to GND.

35) The method as in Claim 34 wherein the first transfer gate comprises:

(a) a PFET with a source, drain, and gate;

(b) an NFET with a source, drain and gate;

(c) wherein the drain of the PFET and the source of the NFET are connected to the input of the first transfer gate;

(d) wherein the source of the PFET and the drain of the NFET are connected to the output of the first transfer gate;

(e) wherein the gate of the PFET is connected to the first control input of the first transfer gate;

(f) wherein the gate of the NFET is connected to the second control input of the first transfer gate;

(g) wherein the first control signal has the opposite phase of the second control signal.

36) The method as in Claim 35 wherein the second transfer gate comprises:

(a) a PFET with a source, drain, and gate;

(b) an NFET with a source, drain and gate;

(c) wherein the drain of the PFET and the source of the NFET are connected to the input of the second transfer gate;

(d) wherein the source of the PFET and the drain of the NFET are connected to the output the second transfer gate;

(e) wherein the gate of the PFET is connected to the first control input of the second transfer gate;

(f) wherein the gate of the NFET is connected to the second control input of the second transfer gate;

(g) wherein the first control signal has the opposite phase of the second control signal.